Advanced Packaging Interconnect Trends and Technology Developments
E. Jan Vardaman, President, TechSearch International, Inc.
Advanced Packaging Market Share

- Advanced Packaging includes BGAs and CSPs, WLPs, and flip chip
- Growing in unit volume and dollar value

Source: IC Insights and TechSearch International, Inc.
Drivers for Advanced Packaging Growth

- Mobile phones
  - More than one billion mobile phones expected to ship in 2007
  - Mobile phones contain an average 15 CSPs, including SiP
  - SiP for digital baseband section, transceiver section, RF section, camera module
  - Drives volumes for stacked die packages and system-in-package (SiP)
- Portable consumer products (digital camcorders, cameras)
  - Digital cameras/camcorders, MP3 players, DVD players, etc.
  - More than 100 million of Apple’s iPods shipped since 2002
  - Thin is in…..drives new package technology developments
- Personal computers
  - PCs highest volume application for PBGAs
- Game machines
  - Growing volumes for PBGAs and CSPs
Sony’s PS3 with BGAs and CSPs

- More than 20 BGAs and CSPs
- Leadframe parts including QFPs

Source: http://pc.watch.impress.co.jp
Apple’s iPod Nano

- At least 7 CSPs on the main board, all wire bonded
- CSPs are underfilled
- 4 Gbit memory package in a TSOP, mounted on a daughter card
- 2 Gbit memory mounted directly on the board

Source: Adapted from Impress Corporation

Source: Apple Inc.
Panasonic P901iTV

<table>
<thead>
<tr>
<th></th>
<th>①</th>
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<th>④</th>
<th>⑤</th>
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<tbody>
<tr>
<td>PKG TYPE</td>
<td>FBGA(L)</td>
<td>FBGA(L)</td>
<td>FBGA(L)</td>
<td>FBGA(L)</td>
<td>FBGA(L)</td>
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<tr>
<td>PIN COUNT</td>
<td>109</td>
<td>257</td>
<td>624</td>
<td>90</td>
<td>376</td>
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<tr>
<td>PKG SIZE (mm)</td>
<td>11.5x13.0</td>
<td>10.0x10.0</td>
<td>13.0x13.0</td>
<td>11.0x13.0</td>
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<td>PKG Thickness (mm)</td>
<td>1.20</td>
<td>1.0</td>
<td>1.20</td>
<td>0.80</td>
<td>1.20</td>
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<tr>
<td>Terminal Pitch (mm)</td>
<td>0.80</td>
<td>0.50</td>
<td>0.50</td>
<td>0.80</td>
<td>0.50</td>
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</tbody>
</table>

Source: TPSS
Apple’s iPhone

- More than 700,000 iPhones sold during the first weekend of product introduction
- Many wire bonded parts, a few WLPs

Source: http://www.embedded.com
Apple’s iPhone

Intel stacked die package

QuickTime® and a TIFF (LZW) decompressor are needed to see this picture.
Apple’s iPhone

- Contains stacked die and PoP
- Samsung PoP with processor in the bottom package and two 512 Mbit SRAM die in the top stacked die package

Source: http://www.embedded.com
Stacked Die CSP Package Growth

- Mobile phone is main growth driver
- Also found in digital cameras and camcorders
- CAGR 9.8%

Source: TechSearch International, Inc
Stacked Die CSPs

- 16 die stack demonstrated, 4-5 die per package common, typically 2 die per package in today’s products
- Typically wire bond, but some gold stud bump (using ball bonder)
Fujitsu F903i Mobile Phone

- 14 CSPs
  - CSPs include FBGA, QFN, and WLPs
  - Renesas processor in a stacked die package
  - Stacked die packages
  - Four MCMs and other LGAs
  - Packages typically wire bond
  - CMOS image sensor camera module with 54 wire bonds

Source: TPSS
Spansion’s Stacked Die in Fujitsu’s F903i

- Two die stacked package
- Hundreds of wire bonds per CSP

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
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<tbody>
<tr>
<td>Marking</td>
<td>98WS768P0GFA006</td>
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<tr>
<td>Body Size</td>
<td>9x13mm</td>
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<tr>
<td>Ball Pitch</td>
<td>0.80mm</td>
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<td>Substrate THK</td>
<td>0.25mm</td>
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<td>Mold Cap THK</td>
<td>0.79mm</td>
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<td>PKG THK except Ball</td>
<td>1.04mm</td>
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<tr>
<td>Bonding Method</td>
<td>Wire Bonding</td>
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<tr>
<td>Die Configuration</td>
<td>2 Dies Stacked</td>
</tr>
<tr>
<td>Die size (Top die)</td>
<td>6.4x7.4x0.1mm</td>
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<tr>
<td>Die size (Middle die)</td>
<td>9.6x5.3x0.09mm</td>
</tr>
<tr>
<td>Die size (Bottom die)</td>
<td>11.7x6.9x0.09mm</td>
</tr>
</tbody>
</table>

Source: TPSS
Stacked Die in Fujitsu’s F903i

- SDRAM on top of 4 die stack
- Two DDR2 memory die mounted on Renesas G1 processor
- Total of 207 wire bonds in memory stack

Source: TPSS
Stacked Die SiP in Fujitsu’s F903i

128Mb M-SDRAM
512Mb DDR2 #1
512Mb DDR2 #2
G1 processor

DAF 1
DAF2
DAF3
Underfill

Source: TPSS
Spansion’s Stacked Die in Fujitsu’s F903i

Source: TPSS
Samsung’s X818 Phone with Stacked Die CSP

- Mobile phone for China market
  - Contains 18 CSPs plus several MCMs
  - Contains stacked die CSPs

FBGA(L) 224pin
- 10.0x10.0x1.20t
- P=0.50
- W/B 1 chip

FBGA(L) 167pin
- 10.5x14.0x1.40t
- P=0.80
- W/B 4 chips

FBGA(L) 25pin
- 3.0x3.0x0.80t
- P=0.50
- W/B 1 chip

Source: TPSS
Samsung’s X818 Phone with Stacked Die CSP

FBGA(L) 100pin
8.0x8.0x1.20t
P=0.80
W/B 2 chips

Source: TPSS
Spansion’s Roadmap for Die Stacking

- Number of die per stack has increased over time, and with it an increase in the number of wires
- Die thickness has decreased
- At the same time, pitch has decreased
Stacked Die Packaging Trends

- Thinner packages
  - From 1.2, 1.4 mm to below 1 mm.

- Higher level stacking
  - From 2, 3, 4 level to 5, 6, 7 level stack

- Multi-function chips
  - From flash and SRAM to including ASIC and logic

- Thinner die
- Lower loop height
- Control of impact when bonding on overhang

- Longer wire length
- Looping sway control
- Thermal control

- Finer pitch
Stacked Die Challenges

- Wafer thinning/die attach
  - Thickness of 75 µm in volume production today
  - Development work with thicknesses of 50 µm in development for both 8-inch and 12-inch wafers
  - Mechanical issues with dicing (handling, chipping, flaking)

- Wire bonding
  - Low loop heights, reverse bonding
  - Smaller diameter wire, longer spans
  - Die to die wire bonding can be complex
  - Die overhang (spacers required for same size die)

- Material selection
  - Substrates need to be thin, but rigid
  - Mold compound selection

- Thermal performance

- Business issues if logic + memory
  - Logistics
  - Testing (KGD)
  - Yield
Package on Package (PoP) in Panasonic’s P902i

- Individual packages stacked on top of each other, typically during board level assembly
- At least 10 major OEMs in handset and digital still camera market adoption PoP
- TechSearch estimates 67 million PoPs were shipped in 2006

Source: TPSS
Amkor’s PoP Options

PoP Deployment

- CABGA, SCSP family
  - low cost

- PS-vfBGA
  - with 2 die stack

- PS-vfBGA
  - with single die

- PS-vfBGA
  - flexible substrate design
  - high density, low cost

PoP Development

- etCSP
  - thinnest profile

- S-etCSP
  - thinnest profile

- SiP stack w/ passives integrated

- PS-fcCSP

- PS-SCSP
  - 2 die stack

- PS-etCSP
  - full cavity
  - thinnest profile
  - stacked die

- PS-fcCSP
  - high I/O count

Source: Amkor
SiP Growth

- Cell phones
- PDAs
- MP3 players
- Cameras
- Computers
- Automotive
- Medical
- Industrial
- Defense
- Aerospace

SiP is a functional system or subsystem assembled into a single package.

- Utilizes combination of advanced packaging such as bare die (wire bond or flip chip), CSP, stacked package, stacked die
- CAGR of 15.9%

Source: TechSearch International, Inc.
ASE Examples of SiP for Mobile RF

- Examples of PA (with antenna and switch), Transceiver, Front-End Module, DCR, SPR, BT, WLAN
- Module package size ranges from 3mm x 3mm to 13mm x 13mm
- Package thickness from 0.85 to 1.8 mm
- Die including silicon (min. 75µm thick), SiGe, GaAs HBT, pHEPT, CMOS, SAW/BAW filter
- Fine pitch wire bond 45 µm bond pad pitch

Note: DCR (Direct Conversion Receiver), SPR (Single Package radio), pHEMT (Pseudomorphic High Electron Mobility Transistor), HBT (Hetero-junction Bipolar Transistor), CMOS (Complementary meta-Oxide Semiconductor)
SiP Configurations in Mobile Phones

- RF section
- Baseband section
- Camera module
- PA module

Source: TPSS

Source: Amkor

Source: Skyworks
Future 3D TSV Camera Modules with Gold Stud Bump

Stud bump made of Au wire

Au stud bump

Al wiring

Cu plated via

RIE or Laser Drill

Stacking cross section

Source: Hitachi
Wire bonding remains the “mainstay” of the industry

- Bumped die includes flip chip, wafer level packages, gold bump driver ICs
Why Doesn’t Flip Chip Dominate the Interconnect World?

- Flip Chip is used where needed, for performance or pad limited designs mostly, but in some cases form factor
  - Continued advances in wire bond technology
- Flip chip substrates are typically more expensive than wire bond substrates
  - Wire bond designs typically routed in four layers
  - Flip chip substrates are more complex, route bumped die with fine pitch
  - Flip chip often requires build-up substrates with lower yield, more expensive material sets, greater complexity
Why Doesn’t Flip Chip Dominate the Interconnect World?

- Many companies have found that flip chip assembly is typically more expensive than wire bond
  - Flip chip substrate shortage in 2005 increased substrate prices, with current overcapacity substrate prices are falling again
  - Intel has twice delayed the move from wire bond to flip chip for the ICH chipset (Southbridge), current delay shifts flip chip adoption out to 2009
  - Estimated assembly cost for wire bond vs. flip chip in large die size 17mm x 17mm found flip chip assembly was 30% more expensive than wire bond (even without consideration of substrates)
Wire bond pitch in actual production has become finer and finer over time, trend continues.

Source: TechSearch International, Inc.
**Bond Pad Over Active I/O**

- LSI developed the industry’s first wire bond over active I/O technology (Pad on I/O™) for copper/low-k
- Allows the extension of wire bond technology to deep submicron CMOS designs in 130nm and 90nm nodes that are typically pad limited
- Placing wire bonds over the active I/O saves die area and does not affect metal routing and interconnect
- Can be used for in-line or staggered pad designs (27µm effective)

Source: LSI
New Developments in Low Loop Height Wire Bonding

- Specially designed for stacked die applications
- Highly accurate and consistent loop profiles
- Improved loop linearity and stability
- Higher bond test results

Source: K&S
ASE’s Wire Bonding Capability

- **Long length capability**

<table>
<thead>
<tr>
<th>Max. Wire Length (MWL)</th>
<th>Wire Diameter</th>
<th>Bond Pad Opening</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.8mm (150mil) &lt; MWL ≤ 4mm (160mil)</td>
<td>30um (1.2mil)</td>
<td>B.P.O. ≥ 80(um)</td>
</tr>
<tr>
<td>3.5mm (140mil) &lt; MWL ≤ 3.8mm (150mil)</td>
<td>28um (1.1mil)</td>
<td>B.P.O. ≥ 63(um)</td>
</tr>
<tr>
<td>3.3mm (130mil) &lt; MWL ≤ 3.5mm (140mil)</td>
<td>25um (1.0mil)</td>
<td>B.P.O. ≥ 53(um)</td>
</tr>
<tr>
<td>3mm (120mil) &lt; MWL ≤ 3.3mm (130mil)</td>
<td>23um (0.9mil)</td>
<td>B.P.O. ≥ 43(um)</td>
</tr>
<tr>
<td>MWL ≤ 3mm (120mil)</td>
<td>20um (0.8mil)</td>
<td>B.P.O. ≥ 40(um)</td>
</tr>
</tbody>
</table>

- **Die to Die Bonding**

  65 µm bonding pad pitch Min.
  55 µm bond pad open Min.
ASE’s Wire Bonding Capability

✓ **Forward bond-standard**

   - **Min. loop height : 75µm (20µm wire)**

✓ **Reverse bond**

   - **Min. loop height : 50µm (20µm wire)**
Microbonds X-Wire™ Technology

- X-Wire™ is a coated wire bond technology
  - Proprietary process developed to coat wire
- X-Wire™ allows greater design flexibility:
  - Relax tight wire bonding rules and corner pad rules
  - Relax loop profiling and wire connection violations
  - Allows crossing, touching wires and long wires
Conclusions

- Advanced packaging continues to grow in units and revenue
  - IC package subcontractors improve revenue growth with advanced package assembly
- Advanced packaging ≠ FC
- Wire bond accounts for 90% of IC packages shipped in 2006
- Advanced packaging includes BGAs, CSPs, flip chip, and wafer level packages
  - Wire bond accounts for 67% of all advanced packages
  - Strong unit volume growth in a variety of packages including stacked die, SiP, BGA, and all types of CSPs
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