

Assembly Using X-Wire™ Insulated Bonding Wire Technology

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Abstract

As the semiconductor industry continues to migrate towards higher pin count, finer pitch, multi-row and multi-stack devices; wire bonding becomes an increasing challenge for today's advanced packaging processes. Insulated bonding wire technology, known as X-Wire™, has been identified on the 2006 ITRS Roadmap for Semiconductors [1], as a viable, cost-effective solution to enable complex package designs, enhance package performance, and improve the yield of high-density packaging.

In order to successfully implement insulated wire bonding, low cost integration into the existing packaging assembly infrastructure is of utmost importance. In particular, it is a requirement that the insulated bonding wires demonstrate wirebonding and package assembly performance which meets industry standard wire bond package test specifications when used on existing wirebonding and packaging assembly platforms. This paper will discuss various methods, techniques and processes developed to date that allow insulated wire packages to be assembled with high yield and reliability using current production equipment. Proper capillary selection and wire bonder setup, as well as correct use of bond parameters, loop parameters, plasma parameters and other advanced wirebond and packaging techniques will be highlighted.

Background - System Packaging Selection

IC packaging is often described as the linkage between the silicon and the system. In layman's terms, electronics packaging can be described as the process of connecting chips together to create an electronic system. The ultimate technical goal is to deliver the highest performance chip function to the end-user at the lowest cost; however, limitations in packaging and chip manufacturing technology create a 'drag' in the system which reduce the final performance to the user. These limitations are the compromises that chip designers and systems architects have had to make to accommodate the shortcomings in the interconnection (packaging) technology available.

Chip Level Interconnection

An important first step in electronics packaging interconnections are the chip-level, (also called first-level) interconnects. This interconnect will dictate to a high degree how much performance can be achieved from a chip. Performance is critical; however, an IC product manager cannot consider performance in isolation to other economic factors. Important considerations in a full benefit/cost tradeoff analysis can be grouped into the following categories: (1) Cost, (2) Performance, (3) Size/Density, and

(4) Time-to-Market. Packaging technologies are typically evaluated on this basis.

Although many types of first-level interconnection technologies exist to connect chip-to-chip, and chip-to-substrate, two primary methods continue to dominate the industry: (1) Wire bonding & (2) Flip Chip (a form of Wafer Level Packaging), with wirebonding holding greater than 90 percent of the market. Over time, niche technologies such as TAB (tape-automated-bonding) and more recently, through-silicon-via (TSV), have emerged to provide alternate solutions to specific interconnection challenges.

Insulated Wire Bonding

The semiconductor industry has been seeking a viable insulated wire bonding solution for almost as long as wirebonding technology has been available [2,3]. The benefits of insulated wire bonding have been well known and clear for many years:

With respect to a full benefit/cost tradeoff analysis, insulated bonding wire provides:

- 1) Cost:
 - a. The ability to use the lowest cost manufacturing infrastructure, which is wirebonding.
- 2) Performance:
 - a. The ability to allow more interconnections per unit area at the chip level, enabling low cost 'die shrink' chips and reducing bond pad layout limitations.
 - b. The ability to connect chips directly together for highest bandwidth connection, eliminating layers of chip, substrate and board level wiring and allowing flexible routing.
 - c. The ability to bring signal and ground wires very close together to minimize inductance.
- 3) Size:
 - a. The ability to place chips tightly together, known as 'brick-wall', not requiring a wire-bond fan-out or keep-out area.
 - b. The ability to connect stack dies directly and flexibly in a wide variety of configurations.
- 4) Time-to-Market:
 - a. The ability to use existing chips immediately without additional chip or wafer processing.
 - b. The flexibility to be applied on a wide range of applications

Because of its flexibility and cost effectiveness and because it leverages a significant amount of proven human capital, wire bonding is the dominant technology in the semiconductor packaging industry, used in over 90 percent of all IC packages. Prior to insulated wire bonding, previous limitations to wirebonding have been that the interconnections have been confined to the perimeter of the chip, and as chip I/Os have increased this has created a need to develop technologies which have area array capability, i.e., chip I/Os which are not restricted to the perimeter. A secondary concern with wirebonding had been inductance of long and parallel wires; which can be alleviated using crossed and closely packed insulated wires. Copper wirebonding, both insulated and non-insulated is also gaining prominence for performance and cost advantages, helping to keep wirebonding at the forefront of the lowest cost/highest performance I/O battleground.

Wafer Level Packaging & Flip Chip Technology

Wafer Level Packaging Technology is an emerging interconnection technology for the IC packaging industry, generally referring to a technique in which bumps applied directly to a wafer, after which the wafer is diced into individual ICs. Wafer level packaging is used in applications requiring small form factor, high density and/or low-inductance. Flip chip can be cost/benefit effective for wiring out very high I/O chips (> 1000) and high frequency applications with similarly low inductance. In relation to wirebonding, the commodity infrastructure for wafer level packaging and flip chip remains in the early stages, as indicated by its relatively higher cost; particularly at low-to-medium volumes.

Flip chip does offer some technical advantages over bare wire bonding for very high I/O, high speed devices, but at high cost compared to the existing wire-bonding infrastructure currently in place. Flip chip for high I/O single-chip packages also competes with advances in system-on-a-chip (SOC) technology, resulting in an overall chip I/O reduction in very high pin count devices. Wire-bonding offers the most flexible and cost-effective interconnection method, particularly where it embraces advanced materials and will be further extended by advances in system-on-a-chip.

Packaging Cost - the Final Arbiter

In the semiconductor packaging industry, where economic improvement is measured in fractions of pennies, cost ultimately rules. Costs relative to packaging technology selection can be considered in two main categories: (1) *Infrastructure adoption costs*, and (2) *Per-Unit scaling costs*.

Incremental Infrastructure Adoption Costs:

With respect to adoption cost, it is clear that wirebonding is the preferred platform, because of the extensive installed base of equipment, materials and human capital as well as interconnect flexibility. It cannot be overstated that a key decision point for the product manager, CTO and assembly house is to increase I/O capability *at the lowest possible*

incremental cost. An example ranking of incremental adoption costs of selected packaging technologies is typically considered to be:

- (1) Wirebonding (including insulated wire)
- (2) Wafer Level Packaging & Flip Chip
- (3) Tape Automated Bonding (TAB)
- (4) Thru-Silicon-Via (TSV)

Per-Unit Scaling Costs:

A recently completed study by Yole [5], provides a type of methodology for comparing per-unit, scaling costs of the various packaging technologies. The comprehensive 250 page report, on the subject of 3D packaging alternatives, examines technologies such as bare (i.e. not insulated) wirebonding, flip chip and package-on-package (POP), in comparison to a new approach called through silicon via (TSV). The cost per interconnect on a wafer basis, for first-level interconnect alternatives, is plotted on a chart. For reference purposes, a 9x9mm die is assumed, having 385 die per wafer. Therefore, to calculate and compare I/O per chip, one can divide wafer interconnects by 385, per Figure 1, below:

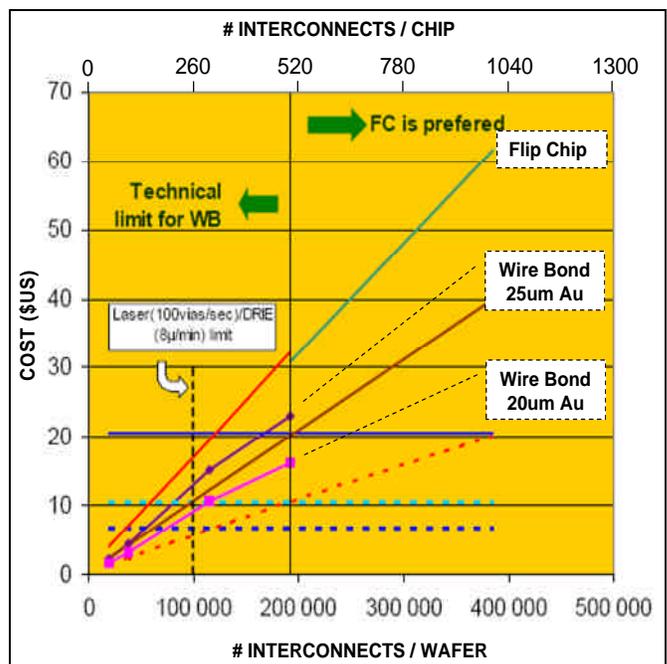


Fig. 1: Interconnection cost of packaging technology. Source: Yole Development

The Yole methodology confirms bare wirebonding as currently the lowest cost IC interconnect technology, relative to flip chip, while the real costs for thru-silicon-via are yet to be determined.

Focusing on the flip chip and wirebond scaling cost graphs, from the above chart, it can be appreciated that the extension of wirebond technology with insulated wire achieves additional interconnect capability increase at a fraction of the incremental adoption cost, once the traditional capability limitations of 2D & 3D parallelism are removed. Hence, the justification for many industry attempts

developing a commercially viable insulated bonding wire technology is clearly understood.

Therefore, considering the cost and benefit together, overall packaging technology selection criteria may be summarized in Table 1:

Table 1: Packaging Benefit / Cost Tradeoffs

	Wire Bond +Insulated	Flip Chip	TSV
Cost	Very Low	Med-High	Very High
Infrastructure	Mature	Early Stage	None
Area array 'on-chip'	Yes	Yes	Yes
Inductance	Low ⁽¹⁾	Very Low	TBD ⁽²⁾
Flexibility	Excellent	Poor	Poor
Reliability	Good ⁽³⁾	Good	Unknown
Direct connect Die-to-Die	Yes	No	Yes
Vertical Stack Die	Yes	No	Yes
Side-by-Side Die	Yes	No	No

Notes: (1) Using insulated wire in shielded signal (co-axial) or crossed bonding layout. (2) Final package to substrate interconnect may be flip chip or wirebond. (3) See Reliability section.

Integration and Assembly of Insulated Bonding Wire into the Wire Bonding Infrastructure

It is important to note, however, that in order to attain the benefit of insulated wire, integration into the existing infrastructure should be backward compatible and relatively straightforward, with low capital cost investment. To that end, it is important to discuss new process windows that are required to successfully implement insulated bonding wire technology.

Package Material Considerations

When evaluating insulated bonding wire for first-level interconnections, the initial considerations are the electrical signal path and primary interconnect interfaces; which are comprised of: (1) the bonding wire, (2) the IC bond pad, and (3) the substrate bond finger.

Insulated Bonding Wire – Diameter and Alloys

Currently the insulated wires that are available for commercial use are gold-based alloys, in diameters of 20um and larger. The proprietary coating process is ‘additive’ meaning that it can be applied to any alloy, including special doped bond wires. This is important, for example, to a customer who has qualified an existing high reliability alloy for longer IMC life. The customer may require the ability of the coating to be applied to the existing qualified wire, which now has an established reliability database. The X-Wire™ coatings have this ‘additive’ property, which can be applied to copper bonding wire, and finer diameters.

IC bond pad structures & pitch

Insulated wire is designed to be applicable wherever bare wire is used for wirebonding. Typical bond pad structures, comprising aluminum metallization with 1% silicon and 0.5 % copper, have been tested and verified. Insulated wire has also been used with sensitive low-k bond pad structures, which can be difficult, even for bare wire.

Substrate Materials

As with standard (non-insulated) wire bonding, the structure of the substrate materials plays a critical role in successful application of insulated wire. For all materials, general guidelines such as consistent and clean bond fingers apply. Insulated wire has been tested on standard organic BGA and leadframe materials. As with normal wire-bonding, each application must be optimized in relation to other assembly constraints, such as: bond pitch, capillary selection, temperature, substrate thickness, looping, and many other factors. A number of techniques for achieving optimized bonding parameters are discussed in the following sections.

Wire Bonding Considerations

With the proper knowledge and correct use of wire bonding parameters, insulated wire bonding can achieve bond strength equivalent to bare bonding wire.

Wire bonder equipment setup

The introduction of insulated wire sometimes requires a simple modification to the wire bonder, relative to the wire grounding point. Typically, a bare wire is grounded through the wire clamps; allowing the high voltage EFO spark which creates the free-air-ball (FAB), to complete its’ return path to ground via the clamps. However, in the case of insulated wire, a grounding point at the end of the wire may be used, in combination with isolation of the wire path. This is to prevent any excessive damage to the coating during FAB formation. Wirebond equipment platforms, such as those made by ASM Pacific & Shinkawa, provide robust end-of-spool grounding as a standard feature. Other wire bonders, offer this feature as a low cost upgrade.

Ball formation and 1st bond

Generally, the ball bonding of insulated wire achieves ball shear values comparable to non-insulated wire bonding; however, optimization of the FAB may be quite different. Insulated wire FAB formation focuses on selecting the correct parameters such as: tail length, EFO current, EFO gap, and EFO time.

A unique attribute of X-Wire™ insulated wire is the characteristic ‘watermelon’ striping pattern on the free air ball, after ball formation, as seen in Figure 2. When done properly, the bottom of the ball is predominantly clean; however, the top surface of the ball contains remnants of split coatings.

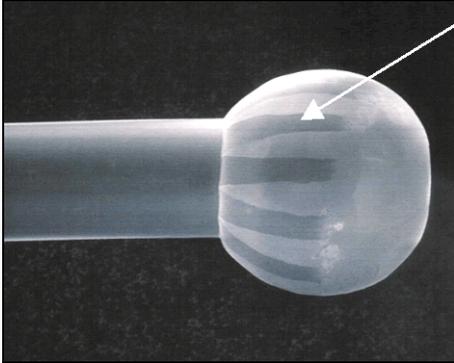


Fig. 2: Free Air Ball (FAB) formation of insulated bonding wire, showing characteristic 'watermelon' striping pattern.

The most notable difference for insulated wire is EFO gap (the gap or distance between the end of the wire and the top of the EFO wand) and EFO current. In general, insulated wire requires shorter EFO gap and lower EFO current relative to bare wire to achieve optimum FAB quality.

Stitch Bond optimization

Second bond or stitch bond, has been the historical weak point of earlier insulated wire technologies [4]. Therefore, much of the development of X-Wire™ insulated wire has been focused on providing a coating material which easily cracks, but only at the second bond, using the available wirebond ultrasonic energy and other second bond parameters, as required.

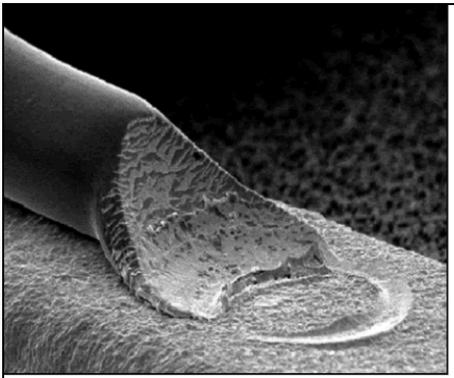


Fig. 3: Stitch bond formation of insulated bonding wire, showing cracking of coating at second bond.

Standard techniques for making a strong second bond have been developed to work with the coating's native ability to crack at the desired time and place. Techniques include: (1) applying high initial bonding force with low ultrasonic energy, (2) applying high initial impact during touch-down, and (3) providing slight scrub motion during second bond to increase the level of coating removal for very high strength bonds, or surface finishes that are difficult to bond.

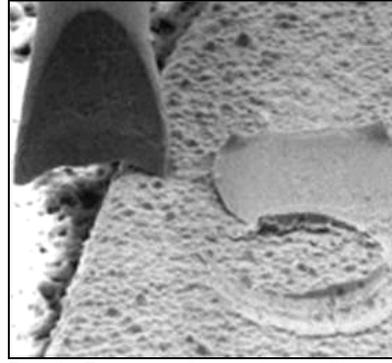


Fig. 4: Example of acceptable stitch bond strength for insulated bonding wire, after peel test. Wire bonding courtesy of ASM Pacific.

Capillary Selection

When selecting a capillary for wirebonding, a number of key geometries to be considered are: hole size (H), chamfer diameter (CD), face angle (FA), chamfer angle (CA), outside radius (OR) and tip surface finish; as shown in Figure 5.

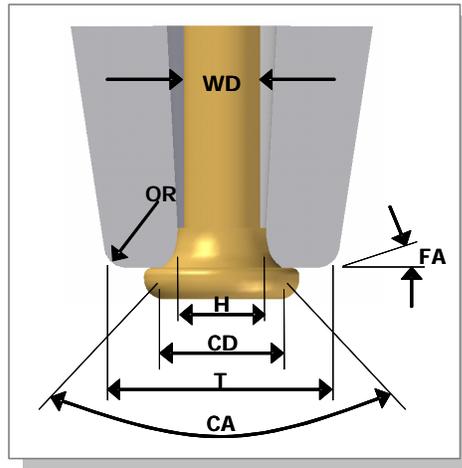


Fig. 5: Capillary Dimensions. Source: SPT

Because X-Wire™ uses stock catalog capillaries, selection of a suitable capillary for insulated wire is similar to bare wire, with a few minor considerations: (1) hole size, (2) outside radius, and (3) tip finish. Unnecessarily large capillary hole size is not recommended. A smaller hole size is preferred for coated wire. The smaller hole does not scrape insulating coating during looping process, even though the X-Wire™ coatings are smooth, with low friction properties enabling good feeding. A smaller outside radius is preferred which maximizes the capillary area in contact with the stitch bond. The capillary tip finish recommended is a matte for insulated wire as compared to a polished surface for bare wire. Again, because the coatings are low friction, the matte finish enables good coupling of the capillary to the coated wire allowing maximum transfer of ultrasonic energy. Recent advancements in capillary surface profiling, allow for even further improvement in a robust stitch bond. Industry testing has confirmed that capillary contamination, a problem with previous industry attempts, is not present with X-Wire™.

IMC Testing

Figure 6 shows 12 optical images of the bottom of etched X-Wire™ bonded balls at time=0. Inter-metallic compound (IMC) coverage on the first bonds formed with X-Wire™ is shown as the dark regions and the percentage coverage of dark region was calculated for each image. The aluminum metallization on the chip pads used in this study was about 0.7 microns thick with 1% silicon and 0.5 % copper. IMC of all the X-Wire™ bonds observed at zero hours exhibits values greater than >75 % coverage.

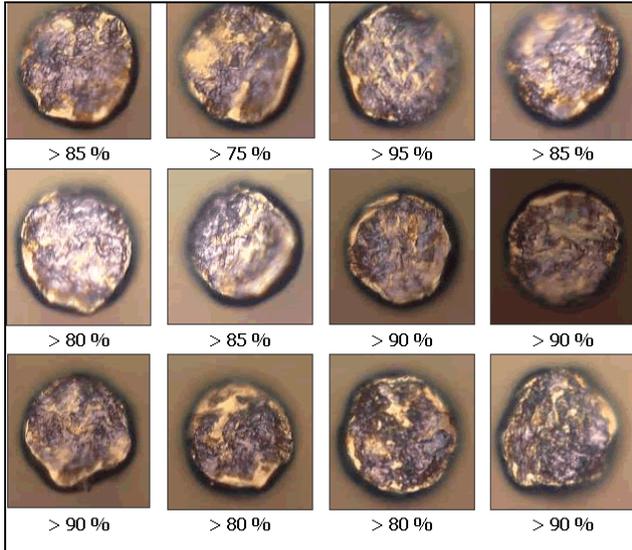


Fig. 6: Inter-metallic (IMC) formation of insulated bonding wire bonds.

Wire Looping

An important attribute of insulated bonding wire is the ability to allow wires to *touch during bonding or during molding as a result of aggregate molding stresses*. This capability alleviates some of the previous requirements of precision looping algorithms and special stiff bond wire alloys, which have been implemented to minimize wire sweep. An example would be the case of a wire which may have required four (4) kinks to cold-work the wire into a shape which keeps it in place between two wire bond tiers on a dense package layout. Forming extra kinks for advanced package designs are significant cycle time adders to overall wirebond throughput. With insulated wire it has been found that, for the same wirebond connection, fewer kinks are required and preferred and overall cycle time is reduced.

Design Rules for Insulated Wire Layouts

Insulated Wire allows wire routing configurations which were previously prohibited, effectively removing restrictions on current bare wire bond design rules. However, insulated wire must be used with care to take advantage of the flexible routing properties while avoiding potential limitations.

Acceptable Bond Layouts

The current version of insulated bonding wire, known as X-Wire 2.0™, allows wire touching and crossing, wire sweeping, long wires and wires beyond current exit angle

restrictions. Examples of the type of acceptable layouts are illustrated in Figure 7, below:

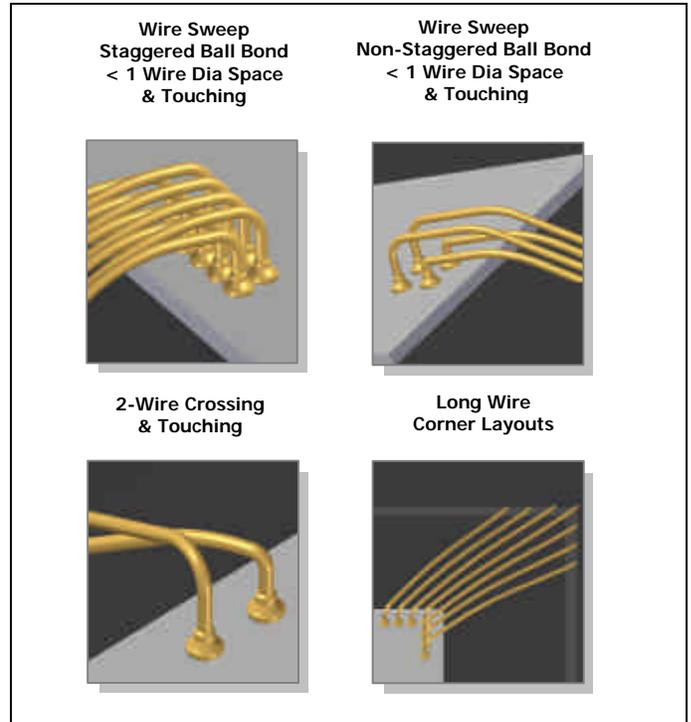


Fig. 7: Example layouts and design rules for acceptable insulated bonding wire packages.

Wire Length

One of the significant immediate capabilities of insulated wire is the removal of the restrictions on wire length. The wire length is now dictated only by the capability of the wire bonder, usually in the range of 7.5mm, for any diameter of wire. This is particularly useful in the case of die shrink revision of on IC, which would retain the ability to use the same package substrate bond finger locations.

Table 2: Allowed Wire Lengths

Wire Diameter (um)	Bare Wire Max Length (mm)	Insulated Wire Max Length (mm)
25	5.0	No Limit
23	4.5	No Limit
20	4.0	No Limit

As mentioned, it is also important to understand layouts which are not currently recommended for insulated wire bonding. Because insulated wire allows wires to touch, wire configurations which are very dense become possible. In these cases, the wires may become trapped in place and exposed to higher than normal stresses from mold flow – particularly filler flow. Therefore, it is recommended that the wires not be trapped, or hard-pinned, during bonding, which should not be the case during normal bonding.

In understanding the current boundaries, two new concepts are defined for insulated wire: (1) Wire pinning, and (2) Wire stacking. Wire pinning occurs when a second wire is bonded down onto a first bonded wire to cause significant

deflection on the first wire, restriction freedom of motion. Wire stacking is defined as three or more wires bonded such that they are in contact, with the all of contact point being within a tight region. Readers will observe that forces which pin the insulated wires which come close to the forces required to cause a good second bond may cause the insulation to be violated to the point of risk of shorting. Future product releases of X-Wire will remove these deflection restrictions allowing even more design layout flexibility. Examples of wire pinning and stacking are shown in Figure 8.

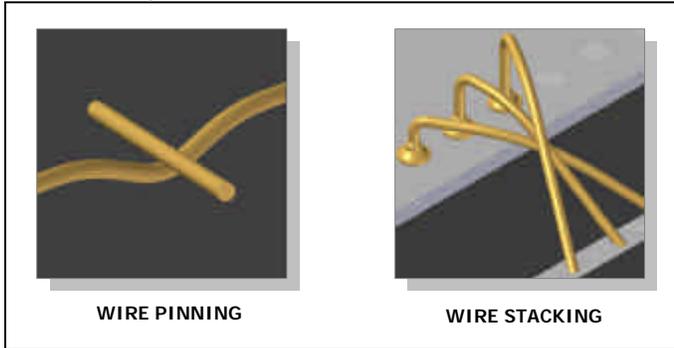


Fig. 8: Examples of future layouts of insulated bonding wire, defined as wire pinning and stacking.

Plasma Cleaning of Insulated Wire

After the wirebonding process, organic packages may be subjected to a plasma cleaning step prior to transfer molding. This step is implemented to clean activate the substrate surface which will promote adhesion of the mold compound and reduce the risk of mold-to-substrate delamination. (X-Wire™ has been tested to confirm a lack of delamination in molded X-Wire™ packages), Therefore, it is important to find plasma recipes and configurations which are compatible with the coatings on the insulated wire.

Through various studies and experiments, it has been found that for insulated wire, pure Argon gas is preferred over other commonly used gas mixtures, such as argon-oxygen or argon-hydrogen. Alternate gases are also currently in development to further expand the process windows for insulated wire compatibility.

A secondary important factor is the shelf configuration and uniform distribution of plasma. Due to the inherently unstable nature of plasma energy, it is found that in some cases the plasma may be not evenly distributed within a large chamber. In order to minimize this effect, it has been found there are preferred shelf configurations to smooth out the plasma distribution and minimize ‘hot’ spots.

In-line plasma processing systems, such as the I-Trak™ from March Plasma, are becoming a popular alternative to batch processing. Such systems allow individual strips to be shuttled in and out of the plasma station, via automated strip handling conveyors. From a process standpoint differences are the small size of the chamber, and the shorter duration of plasma exposure. The small chamber size allows for a more

uniform plasma energy distribution across the strip, which is preferred.

Transfer Molding of Insulated Wire

As mentioned previously, insulated wire provides the benefits of allowing wire touching without the risk of shorting, when used correctly. The design rules of the previous section providing guidelines for recommended layouts should be followed for the current version of X-Wire™ insulated wire, release 2.0. Future roadmap releases will expand the bonding deflection and other process windows.

In terms of molding compound compatibility, insulated bond wires have been tested with the most popular mold compounds from Nitto Denko and Sumitomo. Green compounds have also been tested and are highly recommended.

In terms of process conditions, it is advised to follow standard procedures currently in place for high yield molding. Insulated bonding wire is coated and prevents shorts due to wire sweep; however, it is not recommended to increase mold transfer pressures and lower transfer times beyond what is the norm for bare wire.

Reliability Testing

A range of reliability testing has been performed on X-Wire™ insulated wire by IDM, assembly sub-contractors and supply chain companies. The insulated wire has shown to have high reliability per JEDEC standard specification. A few examples of typical testing, and results for insulated wire, are shown below:

Table 3: Insulated Wire Package Reliability

	Assembly Subcontractor	ASIC Designer
Package Type	MAP BGA	PBGA
Package Size	14 x 14mm	40 x 40mm
Package I/O	409	503
Pre-conditioning	JEDEC L2 / 260C	JEDEC L3 / 245C
High Temp Storage	1000hr @ 150C	1000hr @ 150C
HAST	130C / 85%RH, 100hr Unbiased	130C / 85%RH, 100hr 4V
Thermal Cycling	-65C / +150C 1000 cycles	-55C / +125C 2000 cycles

Conclusion

Selection of packaging technology involves making difficult tradeoffs between economic and technical factors. For newer technologies, infrastructure integration costs are often the deciding factor in the timing of adoption. Insulated bonding wire is a roadmap technology that can potentially lower the integration cost, while providing the desired benefits. New process windows, as described in this paper, must be developed to allow the insulated wire to be used on existing packaging assembly lines.

Summary of Insulated Wire Benefits

1. Leverages proven expertise in wirebonding to achieve lowest cost/highest performance I/O's by facilitating multi row, area array and stacked die
2. Allows use of the Z dimension as well as wasted space created by parallelism of bare wires
3. Conforms to proven bare wire assembly processes with minimal disruption
4. Facilitates movement to finer diameter gold wires as well as to copper interconnects
5. Decreases yield loss due to wire sweep or complex package layouts

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References

- [1] ITRS roadmap 2006. <http://public.itrs.net>
- [2] Susumu Okikawa, Michio Tanimoto, Hiroshi, Watanabe, Hiroshi, Mikino, and Tsuyoshi Kaneda, "Development of a Coated Wire Bonding Technology", IEEE Trans. Comp. Hybrids and Manuf. Tech. Vol. 12, No. 4. pp 603-608, 1989
- [3] Fuaida Harun, Albert Tiu, L.C. Tan, "An Evaluative Study of Insulated Wire in Ultra Fine Pitch Applications", Semicon Singapore, 2004
- [4] Mohd Rusli Ibrahim, Altert Tiu Koo Bee, "Bondability and Reliability for Insulated Wirebonding Process With 63 µm Pitch Capability", IEEE Electronic Packaging Technology Conference, 2005
- [5] 3D IC Report, Yole Development, February 2007